AMENDMENTS TO THE CLAIMS

Please cancel claims 25, 27-31 and 33 without prejudice. The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (previously presented) An apparatus for executing an MMX PSADBW instruction, comprising:

subtractors, for generating packed differences of packed operands of the instruction and for generating borrow bits associated with each of the packed differences;

inverters, coupled to said subtraction logic, for generating an inverse of each of said packed differences;

multiplexers, coupled to said inverters and said subtraction logic, each for selecting as an output said packed difference if said associated borrow bit indicates the packed difference is positive, and for selecting as said output said inverse if said associated borrow bit indicates the packed difference is negative; and

a first adder, coupled to said multiplexers, configured to add said outputs of said multiplexers to generate a first sum and a first carry;

a second adder, coupled to said subtractors, configured to add said borrow bits to generate a second sum and a second carry in parallel with said first adder generating said first sum and carry;

a third adder, coupled to said first and second adders, configured to add said first and second sums and carries to generate a result of the PSADBW instruction.

2. (previously presented) The apparatus of claim 1, further comprising:

an instruction type input, for specifying whether the PSADBW instruction or a multiply instruction is being executed by the apparatus; second multiplexers, coupled to said first adder, configured to provide said outputs of said first multiplexers to said first adder if said instruction type specifies the PSADBW instruction and to provide a first set of partial products to said first adder if said instruction type specifies the multiply instruction; and

third multiplexers, coupled to said second adder, configured to provide said borrow bits to said second adder if said instruction type specifies the PSADBW instruction and to provide a second set of partial products to said second adder if said instruction type specifies the multiply instruction.

3-4. (canceled)

5. (previously presented) The apparatus of claim 2, wherein said third adder is also selectively employed to generate a sum of first and second product results generated by said first and second adders, rather than said result of the PSADBW instruction, if said instruction type specifies the multiply instruction.

6-7. (canceled)

8. (previously presented) The apparatus of claim 1, wherein each of said borrow bits comprises a Boolean zero value if said associated packed difference is positive and comprises a Boolean one value if said associated packed difference is negative.

9. (previously presented) The apparatus of claim 1, further comprising:

a plurality of storage elements, for storing said borrow bits.

10-24. (canceled)

25. (canceled)

26. (canceled)

27-31. (canceled)

32. (canceled)

33. (canceled)

34. (previously presented) The apparatus of claim 1, wherein said third adder comprises:

a fourth adder, for adding said second sum and said second carry and said first sum to generate a third sum and third carry;

a fifth adder, for adding said third sum and said third carry and said first carry to generate a fourth sum and a fourth carry; and

a sixth adder, for adding said fourth sum and said fourth carry to generate said result.